A 60-GHz High Efficiency Monolithic Power Amplifier Using 0.1-μm PHEMT's

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***Abstract*—We report the development of a V-band monolithic power amplifier based on 0.1 μm gate-length pseudomorphic HEMT's. The two-stage amplifier has demonstrated record performance at 60 GHz on the first design pass: 272 mW output power with 9.4 dB power gain and 24% power-added efficiency. The amplifier was designed for high-reliability communications applications, with passivation, good linearity and excellent thermal properties, and has been fabricated on 3-in. wafers with high yield and excellent uniformity—on one typical wafer, consistency of MMIC output power is better than $\pm$0.5 dB with an associated total yield through RF test of 58%.**

I. Introduction

THERE is considerable interest in developing moderate power (1–10 W) transistor-based amplifiers for V-band satellite crosslink applications. These amplifiers have the potential for high efficiency operation with reliability superior to that of IMPATT and traveling-wave tube amplifiers. Pseudomorphic HEMT, or PHEMT, devices have demonstrated peak power-added efficiencies in excess of 40% at 60 GHz [1], and a number of monolithic PHEMT power amplifiers operating at V-band have recently been reported [2]–[6]. However, the highest power V-band MMIC amplifiers have exhibited relatively low efficiencies and operated at high levels of gain compression, compromising linearity. For example, the power amplifier module reported in [7], based on the MMIC described in [4], generated 740-mW output power with 8% power-added efficiency, 11.7-dB gain, and an associated gain compression of more than 9 dB.

In this letter, we report the development of a V-band high-power MMIC amplifier with the highest efficiency reported to date and possessing other properties that should make it well suited to ultra-high reliability communications applications such as satellite crosslinks. The enhancement in performance is attributed to the use of a 0.1-μm PHEMT device structure optimized for 60 GHz operation, as well as accurate device characterization and careful MMIC design.

II. PHEMT Device Design

The PHEMT device is based on a double heterojunction epitaxial layer structure and employs a 0.1-μm T-shaped cross-section gate. Maximum transconductance g_m is typically 600 mS/mm and gate-to-drain breakdown voltage, defined at 1 mA/mm, is 10 V. The active regions of the PHEMT are passivated with silicon nitride, and the MMIC's were fabricated on 3-in. wafers.

The power MMIC is based on a 300-μm gate width transistor cell containing four 75-μm gate fingers, with small, reactive-ion-etched (RIE) via slots under individual source pads. As described earlier in [8], this approach is essential at millimeter-wave frequencies to minimize source inductance, thereby improving gain and efficiency.

Accurate device characterization and small- and large-signal modeling were critical to achieving the first-pass MMIC results reported here. S-parameters of the 300-μm PHEMT cell under both passive and active bias conditions were first measured from 1 to 75 GHz in two setups (a coaxial one for lower frequency and a waveguide test set covering 50–75 GHz) using TRL de-embedding techniques, then a lumped-element equivalent circuit model was developed. Fig. 1 shows the excellent agreement of measured and modeled S-parameters over 1–75 GHz. Based on the lumped-element equivalent circuit model, together with DC measurements, an empirical nonlinear model was developed using the technique described in [9] and implemented with HP-EEsof's Libra Sr.

III. Amplifier Design

A photograph of the two-stage MMIC power amplifier is shown in Fig. 2. The first stage contains a 300-μm gate periphery PHEMT, while two 300-μm devices are reactively combined in the second stage. The impedance transformations required in the input, output and interstage matching circuits were realized predominantly using cascaded microstrip transmission lines with various characteristic impedances. This matching circuit topology is an efficient approach to simultaneously achieve broad bandwidth and reduce process sensitivity at millimeter wave frequencies. The output matching circuit presents the device with its optimum load impedance for highest power-added efficiency, the input circuit provides highest return loss and maximum linear gain, and the interstage circuit is compromised to maintain good gain flatness and deliver sufficient drive to the output stage. To enhance circuit modeling accuracy at V-band, all of the passive elements, including MIM capacitors, RIE vias, step discontinuities and T-junctions, were simulated using electromagnetic simulation tools and verified by on-wafer measurements of test structures incorporated on the MMIC wafers. For example, the measured

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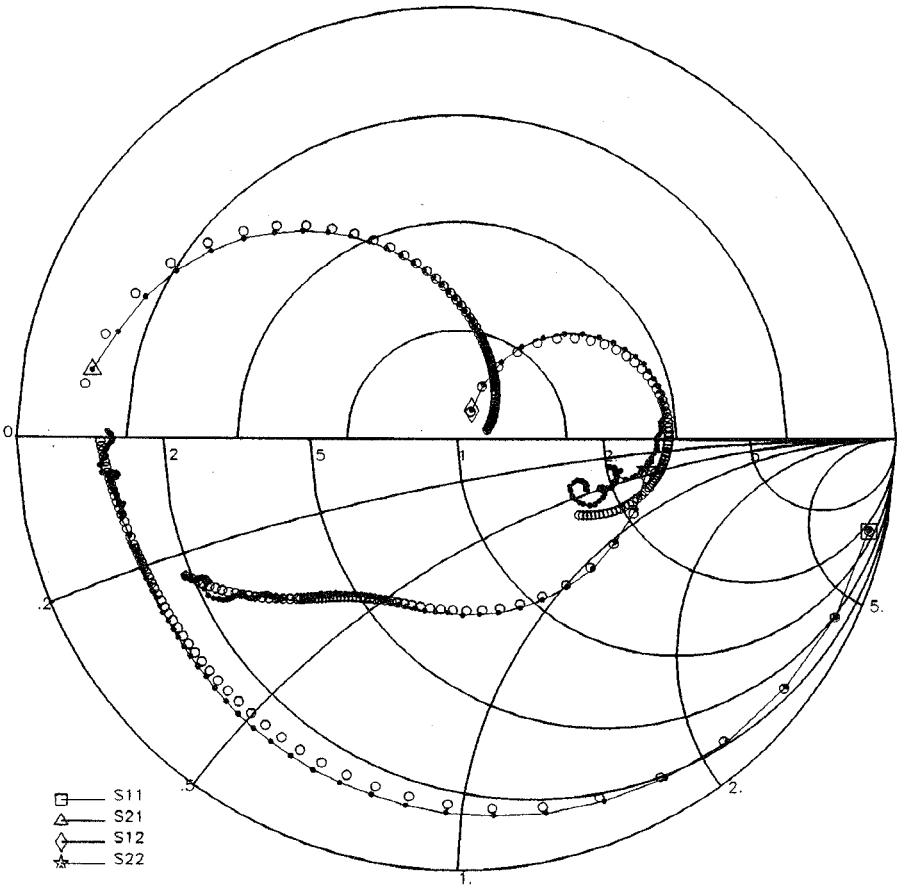

Fig. 1. Comparison of measured and modeled S-parameters of 0.1 μm $\times$ 300 μm PHEMT across 1–75 GHz frequency range. Open symbols are modeled data, S_{21} full scale is 10 and S_{12} full scale is 0.2. Bias conditions are V_{ds} = 4.5 V, I_{ds} = 42 mA.

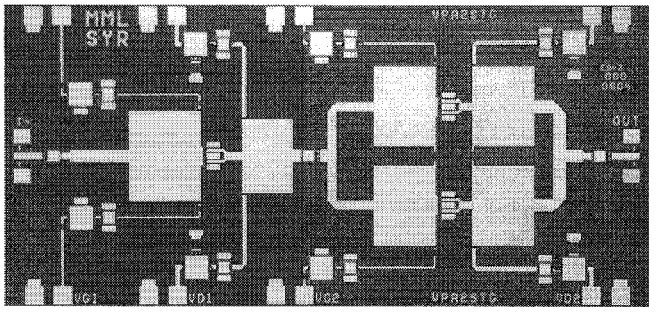

Fig. 2. Photograph of the V-band monolithic power amplifier. The chip size is 3.39 $\times$ 1.61 mm^2.

and simulated S_{21} phase of a series MIM capacitor were found to agree to within less than 2° at frequencies through V-band.

The MMIC was implemented on a 2-mil-thick GaAs substrate primarily to maintain low PHEMT channel temperature for reliability, but the use of a thin substrate also reduces the parasitic inductance of device RIE via slots and RF grounds in the biasing circuitry and allows the realization of microstrip lines of low characteristic impedance. Three-dimensional finite element thermal analysis of the 300-μm PHEMT cell indicates a low normalized thermal resistance of 58.5°C-mm/W, and the corresponding predicted maximum channel temperature rise through the MMIC chip for the operating conditions described below is only 47.6°C.

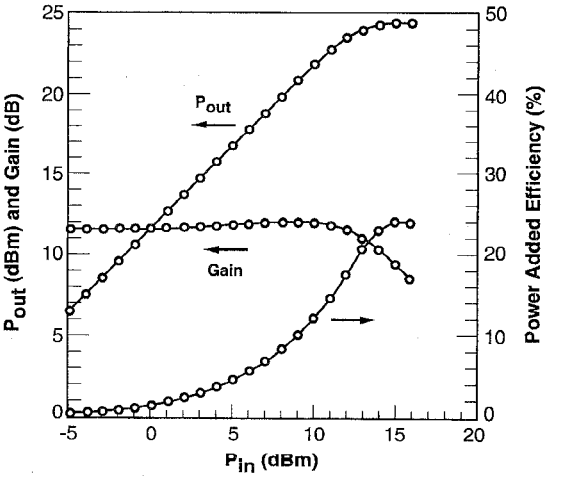

Fig. 3. Measured 60-GHz performance of the monolithic amplifier, operated with both stages at Vds of 5.0 V.

IV. Circuit Performance and Yield

The 60-GHz performance of the two-stage MMIC, measured on-wafer, is shown in Fig. 3. Note that these measurements were made using a WR15 power sensor calibrated with standards traceable to the National Institute of Standards and Technology (NIST). An output power of 272 mW is achieved with 24% power-added efficiency and 9.4 dB power gain. Linear gain is 12.0 dB, and maximum efficiency occurs at

TABLE I
COMPARISON OF REPORTED V-BAND MULTISTAGE POWER MMIC'S WITH GREATER THAN 100 mW OUTPUT POWER

Reference	Substrate Thickness (mils)	Passivation	Number of Stages	Chip Area (mm^2)	Output Power (mW)	Power Gain (dB)	Power-Added Efficiency (%)	Gain Compression (dB)	Power Per Unit Area (mW/mm^2)
This Work	2	Silicon Nitride	2	5.5	272	9.4	24	2.6	50
[6]	4	Not Stated	2	10.7	313	9.0	20	4.8	29
[4]	4	None	2	9.0	482	7.8	14	5.0	54
[4]	4	Silicon Nitride	2	9.0	370	6.7	11	6.5	41
[5]	4	Not Stated	3	2.7	112	8.0	10	8.0	42

2.6-dB gain compression. At 1-dB gain compression (power gain of 11.0 dB), output power is 250 mW with an associated power-added efficiency of 21%.

The performance of this MMIC is compared with that of other reported high power (greater than 100 mW) multistage V-band MMIC's in Table I. As seen in the table, the two-stage MMIC reported in this letter exhibits the highest efficiency reported to date and operates at a reduced level of gain compression, thereby improving linearity (both AM/PM conversion and phase linearity, important parameters for communications applications, improve with reduced gain compression). Furthermore, it is significant that the MMIC performance we present was obtained with passivated devices, since passivation is normally required for high reliability applications such as satellite crosslinks and, as reported in [4], passivation can degrade MMIC performance.

Power per unit area is a useful figure of merit for a power MMIC, representing how efficiently GaAs wafer area is utilized. As seen in the table, our MMIC is comparatively small in size (approximately one-half the area of the MMIC reported in [6]) and hence exhibits relatively high power per unit area. Finally, it is worth noting that the MMIC described herein is the first reported high power V-band MMIC fabricated on a 2-mil-thick substrate in order to minimize channel temperature for improved reliability.

High yield and excellent uniformity of these MMIC's was also observed. On one typical 3-in. wafer, total yield through RF test was 58%, where good MMIC's were defined as those exhibiting output power within a ±0.5-dB range (23.7 ± 0.5 dBm) and having minimum power-added efficiency of 20%.

V. CONCLUSION

A V-band monolithic power amplifier with state-of-the-art performance has been developed using 0.1-μm PHEMT device technology and rigorous device characterization and circuit design techniques. Consistent with satellite crosslink applications, the amplifier is passivated and exhibits record efficiency, good linearity and excellent thermal properties. The combination of excellent performance and high RF yield will allow use of this MMIC in a variety of military and civilian applications at V-band.

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